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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/394,564	09/10/1999	HOWARD THOMAS OLNOWICH	EN997080B	4402

7590 11/29/2001

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EXAMINER	
BATAILLE, PIERRE MICHE	
ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/29/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/394,564	Howard T Olnowich
Examiner	**Group Art Unit**
P. Bataille	2186

☒ Responsive to communication(s) filed on *Oct 3, 2001*

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1 and 31-39* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1 and 31-39* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication dated October 3, 2000. Claims 1 and 31-39 are pending in the application.

Claim Rejections - 35 U.S.C. § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 31-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta et al. (US5,535,116) in view of Hagersten et al. (US5,887,138).

As per claims 1 and 31-34, Gupta teaches a directory-based cache coherency protocol system for a shared memory parallel processing system including a plurality of nodes [Col. 2, Line 64 to Col. 3, Line 4], a shared-memory computer system is forming a plurality of tightly-coupled processing nodes, each processing node having a data processor for executing software instructions, a main memory cache caching global shared data, a processor cache disposed between the data processor and the main memory cache, and a directory memory containing

directory information for each data item assigned to the processing node [Col. 3, Lines 14-26], the directory-based cache coherency protocol system and/or shared-memory computer system further comprising: a multi-stage communication network [general interconnection network 100, Fig. 1 & 2] for interconnecting said plurality of processing nodes [1a-1n, Fig. 2; Col. 3, Lines 10-12]; each said processing node including a one or more caches for storing a plurality of cache lines [22a-22n, Fig. 2; Col. 3, Lines 13-22; Col. 5, Lines 49-57; Col. 6, Lines 6-43]; a cache coherency directory which is distributed to each of said nodes for tracking which of said nodes have copies of each cache line [Col. 3, Lines 4-10, Lines 22-34; Col. 5, Lines 16-33; Col. 7, Lines 7-14].

Gupta fails to specifically teach the features, as added to the independent claims, each processing node including a unique section of shared memory which is not a cache and an adapter for storing changed data to each unique section so that each section contains the most recent data.

However, Hagersten discloses a plurality of processing nodes [12, Fig. 1] interconnected through interconnecting network [14, Fig. 1]; each processing node including multiple processors [16, Fig. 1; 32A-D, Fig. 2], multiple cache memories [18, Fig. 1; 34-A-D, Fig. 2] and local memory [22, Fig. 1; 36A-D, Fig. 2], all local memories or memory portions of the processing nodes collectively form a distributive shared memory which may be accessed in non-uniform memory architecture (NUMA) fashion, i.e. each of said multi-processing nodes includes an addressable portion or local memory modules of the global system memory or sub-divided

portion of the global physical system memory [Col. 9, Lines 31-53; Col. 8, Lines 53-67]; each node of the plurality of nodes shares a shared distributed memory wherein sections or addressable locations of the shared distributed memory are accessible to more than one of the processing nodes [Col. 6, Lines 36-42; Col. 13, Line 1-8; Col. 14, Lines 28-45]; and each processing node having said local memory is capable of storing valid and shared copies of requested ones of data signals stored in the main memory modules [Col. 4, Line 66 to Col. 5, Line 33; Col. 10, Lines 1-14, Lines 53-57; Col. 13, Lines 21-45].

Therefore, it would have been obvious to one having ordinary skill in the art and having the teaching of Gupta and Hagersten before him at the time of the invention to include the feature of each processing node having unique section of shared memory and an adapter for storing changed data to each unique section, as taught by Hagersten, into the shared memory parallel processing and directory-based cache coherency protocol system, as taught by Gupta, because the result would have provided a system with central ordering point enabled to simultaneously receive requests utilizing different protocol and operating speed from all of the sources (processors, Memory, I/O processor) and provided parallel processing while ensuring that the private caches or associated shared memory of each of the processing node are kept consistent or coherent and since every memory block externally cached would minimize any impact on the bandwidth of the common bus, as taught by Hagersten [Col. 7, Lines 22-26; Col. 8, Lines 28-30; Col. 8, Line 61 to Col. 9, Line 10].

As per claim 35, Gupta teaches maintaining a shared memory including a first memory portion for storing unchangeable data and a secondary portion for storing changeable data [exclusive data partition and shared data partition, Col. 10, Lines 7-32]; and said cache coherency directory listing which nodes of said plurality of processing nodes have accessed copies of said cache lines in said second memory portion [Col. 5, Lines 16-33; Col. 7, Lines 7-14].

As per claims 36, Gupta teaches the system wherein said plurality of nodes being operable for reading, storing, and invalidating said shared memory at any other said processing node [Col. 8, Lines 55-67].

As per claim 37, Gupta teaches maintaining data allocation and movement between the processing nodes done explicitly via software written by application programmer or automatically by the operating system [Col.5, Lines 35-43] at a first node a request for access to a memory word for first accessing the cache at said first node and accessing said memory word selectively from a cache line in said memory or a remote memory and storing said cache line to said cache at said first node [Col. 10, Line 45 to Col. 11, Line 37], but fails to specifically teaches a controller configured to selectively access the cache of a first node in response to a request and selectively access the remote node if requested memory word is not in the first node. However, such feature is certainly inherent in Gupta's system since the functions are illustrated. In other alternative, Hagersten teaches a distributed shared memory architecture including a plurality of

processing nodes and distributed shared memory system, the plurality of nodes communicating via a network link coupled there between, and including directories used to identify which nodes have cached copies of data corresponding to a particular address [Col. 9, Lines 35-48, Lines 19-42], the system implements control functions, responsive to a request, for accessing a first processing node of external device and accessing a second external device if the first external device does not cache the requested memory block [Col. 9, Line 66 to Col. 10, Line 16; Col. 11, Lines 8-28]; the system maintaining internode coherency detecting addresses which require data transfer to or from another processing node, i.e. accessed addresses within the address space of a node corresponding to addresses within locations of another processing to maintain consistency [Col. 9, Lines 1-14; Col. 10, Lines 1-27; Col. 16, Lines 18-42; Col. 18, Line 62 to Col. 19, Line 40]. Therefore it would have been obvious to one having the teaching of Gupta and Hagersten before him at the time of the invention, to include the control function of the controller taught by Hagersten within the system taught by Gupta because the result would have provided memory management ensuring the most updated copy is provided to the requestor overcoming the problem of returning the old value, as taught by Hagersten [Col. 4, Lines 51-60].

As per claim 38, the features limiting the invention would have been obvious to any person having ordinary skill in the art because it is known in the art of a number of cache algorithms (most recently used, least recently used, and/or first-in-first-out, etc) providing cache replacement protocol, Gupta teaches the invention specifying that data may be displaced in the form of

replacement when space needs to be allocated to service memory requests [Col. 7, Lines 32-34], a home node initiates replacement of a shared line by simply discards the line and informs the home node to remove the initiating director from the sharing list [Col. 16, Lines 10-24].

As per claim 39, Gupta teaches the system comprising controller operable to send cache update messages updating corresponding cache lines of a changed cache line and for receiving cache line of data from remote nodes for updating the cache [Col. 15, Line 64 to Col. 16, Line 7].

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No.	5,987,506	Carter et al.	Nov. 16, 1999
US Patent No.	5,890,217	Kabemoto et al.	Mar. 30, 1999
US Patent No.	5,394,555	Hunter et al.	Feb. 28, 1995

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

6. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051 (for formal communications intended for entry)

Or:

(703) 305-9731 (for informal or draft communications,

please label "PROPOSED" or "DRAFT");

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tuesday to Friday from 7:30 P.M. to 6:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim, can be reached on (703) 305-3821. The fax phone number for this Group is (703) 308-9731.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

P. Bataille

October 30, 2001

Matthew M. Kim
Supervisory Patent Examiner